AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for the paragraphs that start at the specified page and line number within the present specification:

At page 11, line 16:

Still referring to Fig. 2, the check address generator 124 may be loaded to start error checking from a particular address within the CAM array. Also, the check address generator may be started from a known state, for example, upon device power-up or in response to a reset operation.

At page 40, line 9:

Fig. 24 illustrates an embodiment of an address generator 720 for generating an error scan sequence that is biased toward lower ordered address values. The address generator 720 includes an address counter 721, limit counter 723, compare circuit 725 and flip-flop 727. The address counter 721 maintains an address count that includes at least $\log_2 N$ constituent bits, N being the number of independently addressable storage locations within a CAM array (or CAM block) to be error checked. The address count is output to a first input of the compare circuit 725, and is also output as the check address 155 discussed above. The address counter 721 includes a strobe input coupled to receive an enable signal 126 (e.g., from an instruction decoder as shown in Fig. 1, from another circuit block within a CAM device, or from an external source) and a reset input (RST) coupled to receive a match signal 722 from compare circuit 725. The address counter 721 increments the address count by one in response to a rising edge of the enable signal 126, and resets the address count to an initial address count (e.g., zero, N-1, etc.), if the match signal ~~726~~ 722 is high when a rising edge of the enable signal 126 occurs. The address counter 721 may be designed to self-initialize the address count to the initial address count during device initialization (e.g., power-up), or may initialize the initial address count in response to a system reset signal. For example, the match signal 722 may be logically ORed with reset signal 153, described above in reference to Fig. 1, and the resulting signal provided to the reset input (RST) of address counter 721. Alternatively, reset signal 153 may be provided to another reset input of the address counter 721.

At page 41, line 4:

The limit counter 723 maintains a limit count that also includes at least $\log_2 N$ constituent bits, and which is output to a second input of the compare circuit 725. The limit counter 723 includes a strobe input coupled to receive a delayed match signal 726 from the flip-flop 727, and may also have a reset input (not shown in Fig. 24) to receive a reset signal (e.g., reset signal 153 described above in reference to Fig. 1) to reset the limit counter to an initial limit count (e.g., zero, N-1, etc.). Alternatively, the limit counter 727 may include circuitry to self-initialize the limit count to the initial limit count. In the embodiment of Fig. 24, the limit counter 723 is a modulo counter that increments the limit count by one in response to each rising edge of the ~~rollover~~ delayed match signal 726 until a final limit count is reached (e.g., N-1, zero, etc.), then rolls over to the initial limit count.

At page 45, line 21:

Fig. 26 illustrates an address generator 730 that may be used to generate a biased sequence of row addresses 736 and a linear sequence of block addresses 738. The row addresses 736 may constitute, for example, the row and segment address components of a sequence of check addresses output by the check address generator 383 of Fig. 12. The block addresses 738 may constitute the block select components of the sequence of check addresses output by the check address generator 383 of Fig. 12. The check address generator 730 includes a row address counter 731, limit counter 733, compare circuit 739, flip-flop 727 and block address counter 735. The row address counter 731, limit counter 733, compare circuit 739 and flip-flop 727 operate in the same manner as the address counter, limit counter, compare circuit and flip-flop components of address generator 720 (described above in reference to Fig. 24) to generate a sequence of ~~check~~ row addresses 736 that are biased toward low order address values. The row address counter 731 is similar to the address counter 723 described in reference to Fig. 24, except that, upon reaching a final count value (e.g., N-1), the address counter 731 asserts a terminal count signal 734 (i.e., outputs a logic high level terminal count signal 734). The block address counter 735 responds to assertion of the terminal count signal 734 by incrementing a block address count, thereby incrementing the block address 738. Thus, the block address counter 735 increments the block address after each completed error scan

sequence (i.e., after the row address reaches N-1) so that the biased error scan sequence is repeated for the next CAM block. The resulting sequence of block addresses 738 is a linear sequence, 0, 1, 2, ..., K-1, where K is the number of blocks in the CAM device. The block address count rolls over to an initial value (e.g., zero) after reaching the final count of K-1.

At page 46, line 18:

The ~~check~~ row addresses 736 and the block addresses 738 may be coupled to address decoder 127 shown in Figure 2 to access rows in a CAM array block and CAM array blocks, respectively. For one embodiment, address decoder 127 includes one or more row decoders and a block decoder. Each row decoder is coupled to one or more corresponding CAM array blocks to access rows therein in response to the ~~check~~ row addresses, and the block decoder accesses or selects particular blocks or row decoders based on the block addresses.

At page 50, line 6:

A segment address counter may also be used in the address generator 740 of Fig. 27 either first in line (being clocked by the enable signal 126 and outputting a terminal count signal to the block address counter 737), second in line (receiving the terminal count signal 744 from the block address counter and outputting a terminal count signal to the row address counter ~~731~~741), or last in line (receiving a terminal count signal from the row address counter ~~731~~741).